

<b>Form 1449 (Modified)</b>  <b>Information Disclosure Statement By Applicant</b>  (Use Several Sheets if Necessary)	Atty Docket No.	NEOMP002C2D1
	Application No.:	Unassigned 10/803,783
	Inventor	DEEPAJ S. PUAR et al.
	Group	Unassigned 2824
	Filing Date	Herewith
	Mailing Date	March 18, 2004

**U.S. Patent Documents**

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub- Class	Filing Date
HN	AA	4,191,956	3/1980	Groothuis	345	201	
HN	AB	4,228,528	10/1980	Cenker	365	200	
HN	AC	4,303,986	12/1981	Lans	364	900	
HN	AD	4,330,849	05/1982	Togei et al.	365	181	
HN	AF	4,472,792	09/1984	Shimohigashi et al.	365	189	
HN	AG	4,656,605	04/1987	Clayton	365	52	
HN	AH	4,691,295	09/1987	Erwin	345	188	
HN	AI	4,740,782	04/1988	Aoki et al.	345	205	
HN	AJ	4,812,836	03/1989	Kurakake et al.	345	201	
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HN	AN	5,027,212	06/1991	Marlton et al.	348	512	
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HN	AU	5,353,402	10/1994	Lau	395	162	
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HN	AY	6,346,946	02/2002	Jeddeloh	345	503	
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**Foreign Patent or Published Foreign Patent Application**

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub- Class	Translation	
							Yes	No
HN	BA	0 165 441	12/1985	European Pat. Off.			✓	
HN	BB	0 260 578	03/1988	European Pat. Off.			✓	
HN	BC	0 334 524	09/1989	European Pat. Off.			✓	
HN	BD	0 383 080	08/1990	European Pat. Off.			✓	
HN	BE	0 474 366	03/1992	European Pat. Off.			✓	
HN	BF	0 492 840	07/1992	European Pat. Off.			✓	
HN	BG	0 547 892	06/1993	European Pat. Off.			✓	
HN	BH	3 628 286	02/1988	Germany			✓	
HN	BI	4-211293	08/1992	Japan			✓	
HN	BJ	2 217 066	10/1987	United Kingdom			✓	
HN	BK	2 208 344	03/1989	United Kingdom			✓	

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**Other Documents**

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
HN	BL	Sato et al. "A Wafer-Scale-Level System Integrated LSI Containing Eleven 4-Mb DRAM's, six 64-kb SRAM's, and an 18K-Gate Array," <i>IEEE J. of Solid-State Circuits</i> (1992) 27:1608-1613.
HN	BM	Fujita et al., "TMAP: Integrated Memory Array Processor Toward a GIPS Order SIMD Processing LSI," <i>IEICE Trans. Electron.</i> (1993) E76-C:1144-1150.
HN	BN	IBM Technical Disclosure Bulletin, 35(1A):45-46, June 1992.
HN	BO	NEC Research and Development, vol. 33, No. 4, Oct. 1992, Tokyo, JP, pp. 585-594, "Integrated Memory Array Processor."
HN	BP	IEEE Journal of Solid-State Circuits, vol. 25, No. 1, February 1990, N.Y., pp. 30-35, "A 50 MHz 8 Mbit Video Ram with a Column Direction Drive Sense Amplifier."
Examiner HIEN NGUYEN		Date Considered 6/22/04

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.